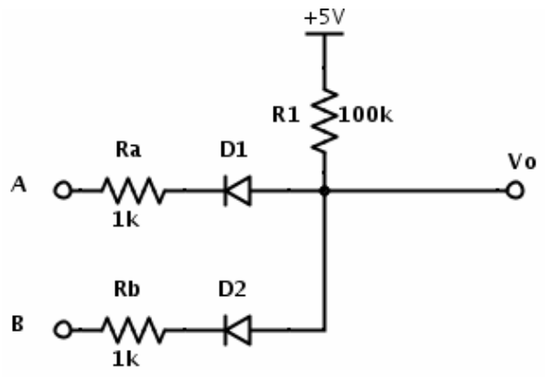
Bangladesh University of Engineering and Technology (BUET)
Department of Computer Science and Engineering (CSE)

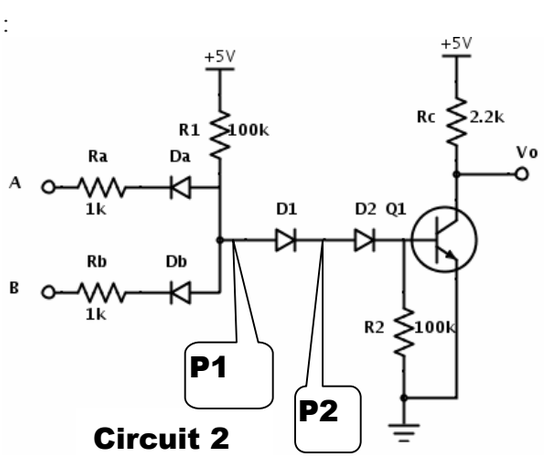
CSE 210 Digital Electronics and Pulse Techniques Sessional

Experiment# 2: Study of a DL *AND* and DTL *NAND* gate

CKT diagram



Circuit 1



Circuit 2

Components Required

1. Transistor BD135	1 pc	3. Resistor 100k	2 pcs
2. Doide 1N4001 or 1N4007	4 pcs	4. Resistor 2.2k	1 pc
		5. Resistor 1k	2 pcs

Procedure:

1. Implement circuit 1.
2. Apply 0v and/or 5v as input to ports A and B.
3. Measure output voltage Vo for all input combinations

4. Implement circuit 2.
5. Apply 0v and/or 5v as input to ports A and B.
6. Measure (i) output voltage Vo and (ii) voltages at points P1, P2 and at the base of the transistor for all input combinations.

Questions:

1. Using experimental data, analyse both the circuits for both positive and negative logic..
2. Why are the diodes D1 and D2 been used? Explain using experimental data.

Report:

Report should cover the following points:

1. Objective
2. Circuit Diagram
3. Experimental Data
4. Calculations if any.
5. Answer to the questions
6. Discussion of the findings